Comparison of soft switched IGBT Inverters

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keywords: RLCD-Inverter, resonant switching, ZCS, ZVS

Abstract:

The net and loadside behaviour of an inverter can be improved by employing soft switching topologies. By reducing switching losses the switching frequency can be increased so that the harmonic distortion can be decreased. Another application for soft switched inverters is the limitation of voltage or current rate of change. Detrimental and not to neglect is the increasing voltage and/or current stress of semiconductors and passive components when resonant operation is used.

In this paper both, the reducing of switching losses and the du/dt limitation are examined.

While in the range of very high power the Resonant Pole topology seems to be interesting, in range of medium power, PWM operated Resonant DC-Voltage Link Inverters seem to be favourable, because apart from the passive components, only two additional switches are necessary to perform soft switching for all employed switches.

In this paper the focus is on two Notching DC Link Inverters with PWM capability. The two topologies have been compared in simulation and an experimental setup for one of them is under construction which will be used to examine the voltage and current stresses of the active and passive components.

Summary:

Overview

Due to the high switching speed in IGBT employed Voltage Source Inverters the voltage and current rate of change in high power applications can reach values up to some kV/µs and kA/µs. As a result there occur EMI problems, a higher stress for the machines winding insulation and HF iron losses. To mitigate this effects additional measures are necessary. The common used method is the use of passive output filters which causes additional power losses and enlarge the volume of the inverter [Bro95]. A second one is to use Soft Gate Drive techniques which means to control the switching process of the IGBT via the gate voltage. In this case there is no change in the power circuitry. The main disadvantage here is the increasing switching power loss. Another possibility is to use multilevel inverters to limit the steps of change in the output voltage. In this paper two soft switching techniques are compared.

In modern IGBT Inverters there is no need for any snubber but because of the switching losses the switching frequency is limited to a few kHz. Increasing the switching frequency is one possibility to improve the line- and/or load-side characteristics of high power converters. The object of efforts in the power-semiconductor technology as well as in circuit design is to increase the switching frequency of high power converters. By introducing soft switching topologies, switching losses may be reduced, but some other drawbacks have to be accepted. For example there is a need for additional measuring equipment, there is a dead time that varies with the load current between the request for the change in the switching state and time of switching. The steering is more complex and last but not least the parameter drift of the passive components, esp. the capacitors, must be taken into account.

In literature there exist many proposals for soft switched inverters, such as the resonant pole inverter, the Parallel Resonant AC Link Inverter, the Resonant DC Link Inverter etc. As a result of a pre-selection, in the range of very high power, the Resonant Pole topology seems to be interesting, while in range of medium power, PWM operated Resonant DC-Voltage Link Inverters seem to be favourable. Resonant DC Link Inverters can be classified as follows:

1.) Inverters, which use a continuously resonating commutation circuit. They need time-discrete gate control strategies, where switching of the power transistors is only allowed at descrete times defined by the resonance of the commutation circuit [Div87]. In this circuit, a considerable amount of energy permanently oscillates between the resonance capacitor and inductor at a frequency of about 50 kHz, which causes losses especially in the inductor. Another problem is a fast change from driving to breaking a machine. Then, despite of a clamping factor of 1.2, the IGBTs are transiently stressed with a voltage of approx. 1.8 U_{dc}. Therefore, the Active Clamped Resonant DC-Link Inverter seems not to be attractive for medium to high power applications.

2.) Inverters using a commutation circuit, which performs a resonant cycle on demand. No (time descrete) restrictions exist for the start of such a resonant cycle [Moh90], [Bor91], [Sal95], [Sul95]. In this paper the focus is on the latter two circuits, as they need only two IGBTs in the commutation circuit.

[Sal95] employs zero voltage switching (ZVS) for all but one transistor, which uses ZCS. [Sul95] uses ZVS for all transistors. These two circuits allow to limit the voltage rate of change in the machines line-to-line voltages.

At first, the two topologies have been simulated using ideal switches and the critical voltage- and current-stress on the devices has been pointed out. Then, some semiconductor effects like rise and fall time or tail current where taken into consideration in a simplified way.

The circuits has been simulated and compared under the aspect of reducing the switching losses, stress of active and passive components and possibilities to limit the voltage rate of change in the output voltage.

Finally, an experimental set-up for the most promising solution is under construction now and measurements will be included in the final paper.

Principle operation

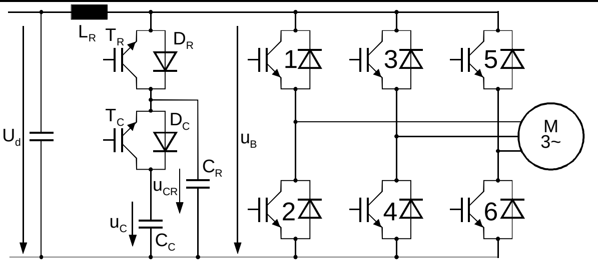

Fig. 1: ZVS for most IGBTs [Sal95]

The circuit shown in Figure 1 provides ZVS for the IGBTs in the inverter-bridge and T_C, T_R is switched off under ZCS conditions. The capacitors C_C and C_R are charged up to $1,2U_d$, the capacitance of C_c is about 100 times C_R. To trigger the resonant cycle the IGBTs in the resonant circuit T_C and T_R are turned on simultaneously, the voltage u_B is clamped to the capacitor voltage u_{CR}, so there is a step increase in the voltage to $1.2U_d$. A low frequency resonant oscillation determined by L_R and C_C starts. When i_{TC} reaches the level I_{TP}, the IGBT T_C is turned off, the current in T_C commutates to C_R and discharges it in a high frequency oscillation. This fast discharging of C_R determines the maximum voltage rate of change in the output voltages. By turning off T_C the voltage u_B is clamped to the capacitor voltage $u_{CR.}$ When u_B reaches zero the IGBTs in the bridge can be switched under ZVS conditions within a short period of time which is determined by the conducting state of the diodes $D_1..D_6$. To restore the capacitor charge of C_R and C_C both IGBTs of one inverter leg are turned on together for a short time before the new switching state is set. This time is determined by the charge flowed out the capacitor C_C. When the new circuit state is set the capacitors C_R and C_C are charged up to $1,2U_d$ again. The maximum rate of change in the machines line-to-line voltages is determined by the capacitance of C_R and the choice of the trip current i_{TP}. To limit du_C/dt the capacitance of C_r must be enlarged or i_{TP} must be lowered to a minimum which is necessary to discharge C_R to zero.

The resonant circuit introduced by Sul is shown in Figure 2. In the steady state the resonant tank energy is zero, T_{R1} is closed and T_{R2} is open. The snubber capacitors provide ZVS mode switch off of the bridge IGBTs, independent of the resonant circuit. By turning T_{R2} on, a resonant cycle is started. The current in T_{R1} increases to feed energy into the resonant tank. As soon as i_L reaches I_{TP1} T_{R1} is opened and u_B is clamped to the snubber capacitor voltage u_C. i_L then discharges the snubber capacitors in a high frequent oscillation which determines the maximum voltage rate of change. When u_B reaches zero all the IGBTs in the inverter are turned on under ZVS conditions. i_L changes its direction and when it reaches the negative value I_{TP2} the new circuit state is set. The snubber capacitors are charged up to U_d and T_{R1} is turned on under ZVS conditions. C_R is discharged via D_{R1} and D_{R2}. When u_C reaches zero L is demagnetised via D_{R1} and D_{R4}.

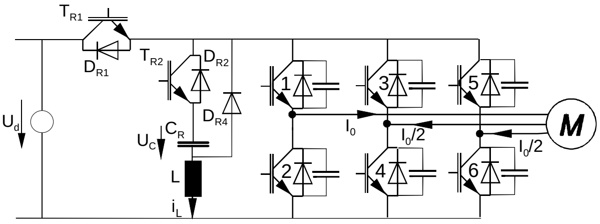

Fig. 2: ZVS for all IGBTs [Sul95]

Experimental setup

The circuits mentioned above have been simulated. Comparing the simulation results, we decided to build up an experimental set-up, based on [Sul95] for the following reasons:

- Using ZVS to perform soft switching allows to limit the rate of change in the machines line to line voltages
- During a resonant cycle in [SAL95] the voltage u_B rises up to $1.2U_d$, so there is a rise in the machines voltages too.
- In order to achieve ZVS, an extreme precise gate timing seems to be necessary with [Sal95]. [Sul95] is less sensitive in this respect.
- The snubber-capacitors allow a ZVS turn off any time irrespective of the link voltage
- In [Sul95] the IGBT T_{R1} can be used to separate the inverter-bridge from the DC-link in case of an fault.

- In [Sul95] the resonant tank energy is zero in steady state, so there is no need for controlling it
- Overvoltages produced by parasitic inductances are damped by the snubber capacitors.

Simulation Results

Figure 3 depicts the simulation results using the resonant circuit from Sul shown in figure 2. In this simulation a change from voltage-vector {1} to {2} is examined. The load-side currents are assumed to be constant for the time the resonant operation takes. The resonant operation is triggered at t_0. At t_1 T_{R1} has to switch off a current that is about two times the load-current in this example. This is a disadvantage of [Sul95], but this problem can be solved by using two parallel IGBTs to realise T_{R1}. The maximum current of the IGBTs 1-6 is close to the maximum load current. The maximum voltage rate of change which occurs in [SUL95] can be seen in figure 3 between t_1 and t_2 when the snubbers are discharged. The snubber charging current is smaller so between t_4 and t_5 du/dt is smaller.

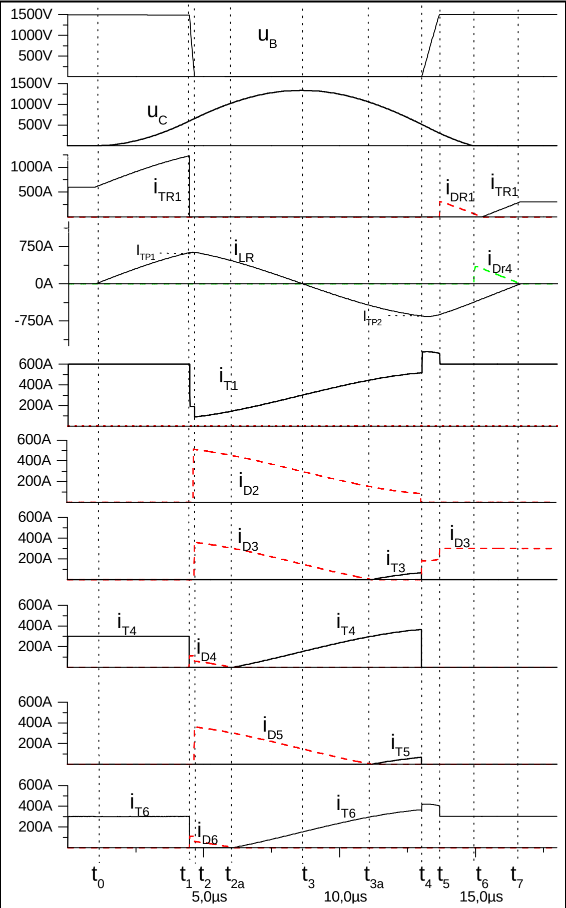

Fig. 3: Commutation process in [Sul95]

As long as (in the mentioned case) D_2 conducts the inverter bridge transistors can be switched under ZVS conditions. At the end of the resonant cycle the diode D_{R4} feeds the surplus of resonant tank energy back into the DC-link.

The simulations have shown that limiting the voltage rate of change and reducing the switching losses are two opposed aims. For low switching losses a large du/dt in the resonant capacitor is necessary, so that limiting du/dt is only sensibly if the switching losses are not to be minimised.

The final paper will present experimental results using a resonant circuit (1.5KV, 150A) according to [Sul95] and discuss the differences of the mentioned circuits in more detail.

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