# Advanced Control Scheme for a Single-Phase PWM Rectifier in Traction Applications

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**Abstract**

This work presents an advanced control scheme for a single-phase PWM rectifier. The controller consists of the PR (Proportional-Resonant) controller using the double sampling strategy, namely, dual update scheme, and the delayless feed-forward compensator. The PR controller is capable of regulating a sinusoidal line current without an additional prediction or an extremely high control gain under a medium switching frequency (0.5~5kHz). The *dual update scheme* is the method performing the sampling and the control calculation twice in a switching period, which reduces the control time delay significantly and enables us to extend the maximum allowable control bandwidth without increasing the switching frequency. The proposed feed-forward compensator uses the estimated and one-step predicted value of the source voltage and the source current to avoid the adverse effects caused by the one-step delay, measurement noise, and harmonic component of the source voltage in the feed-forward compensation process. A very fast phase angle estimator is also presented, which is capable of estimating the phase angle and the frequency of the source voltage even under a highly distorted line voltage condition or a sudden amplitude, phase angle or frequency changing condition. The feasibility of the proposed control scheme is confirmed by simulation study.

Area of interest : Industrial Power Conversion Systems Department (Industrial Power Converter Committee)

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## I. INTRODUCTION

An example configuration of a PWM single-phase rectifier is shown in Fig. 1. The source power is supplied through a pantograph and a transformer. The leakage inductance of a transformer plays a role of an inductor filter. In this work, we present an advanced control scheme for a single-phase PWM rectifier, which consists of the PR (Proportional-Resonant) controller that is able to regulate a sinusoidal line current without an additional prediction or an extremely high control gain, the double sampling strategy, namely, *dual update scheme* that can reduce the control time delay significantly and enables us to extend the maximum allowable control bandwidth without increasing the switching frequency, and the delayless feed-forward compensator that avoids the adverse effects caused by the one-step delay, measurement noise, and harmonic component of the source voltage in the feed-forward compensation process.

## II. PROPOSED CONTROL SCHEME

### A. Very Fast Phase and Frequency Estimation

When the source voltage changes in a step manner, the normal phase angle detector such as a phase locked loop(PLL), *etc.* typically generates a significant phase delay and results in a sluggish response. This work proposes a very fast and robust (insensitive) phase angle estimation algorithm that operates well even under a sudden voltage changing conditions, and a frequency estimation scheme to accommodate a frequency varying environment. The phase angle estimation algorithm is derived from the *weighted least-squares estimation* (WLSE) method with the *covariance resetting* technique. With the proposed estimation method, one can find the phase angle, the frequency and the fundamental component of the source voltage within a few sampling periods, even when both the phase angle and the amplitude change in a step manner.

A single-phase voltage $E_s$ is given by

$$
\begin{aligned}
E_s(t) &= \overline{E}\cos(\omega t + \phi), \\
&= E_d \cos\omega t - E_q \sin\omega t, \quad (1)
\end{aligned}
$$

where $\overline{E}$ is the amplitude, $\omega$ is a constant angular frequency, $\phi$ is the phase angle, $E_d = \overline{E}\cos\phi$, and $E_q = \overline{E}\sin\phi$. By applying the WLSE method to (1), the estimation $\hat{E}_d$ and $\hat{E}_q$ are obtained from $E_s$ [2]. The phase angles estimation is obtained from $\hat{E}_d$ and $\hat{E}_q$ such that

$$
\hat{\phi}(t_i) = \text{atan2}(\hat{E}_q(t_i), \hat{E}_d(t_i)), \quad (2)
$$

where atan2 is the arc-tangent function.

To enhance the tracking speed of the phase angle jump caused by sudden change of the voltage, the *covariance*
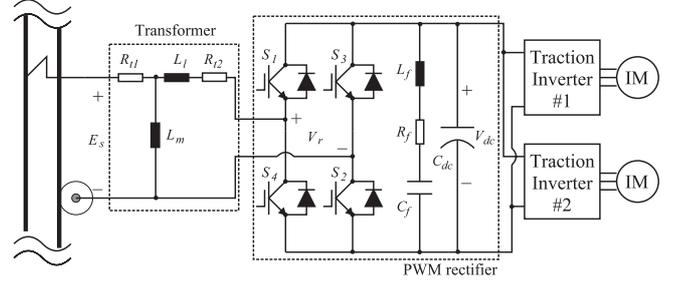


Fig. 1. Structure of a single-phase PWM rectifier for traction applications.
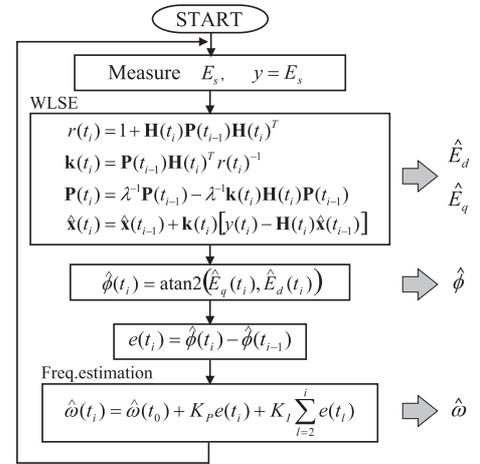


Fig. 2. Flowchart of the proposed phase and frequency estimation algorithm. It can find the phase angle of the source voltage without a delay even under a sudden voltage change condition.

*resetting* technique is adopted. That is, when a sudden change of the voltage is recognized, the covariance of the WLSE is reset with a large value, which is equivalent to enlarge the convergence gain, then the estimation speed is increased [3]. This technique enables the estimator to track a step changed signal within a few sampling periods.

The proposed phase angle estimation algorithm can be extended to the estimation of $\omega$, when the frequency varies. When the frequency estimate $\hat{\omega}$ is not equal to the real frequency $\omega$, the estimated phase angle $\hat{\phi}$ varies such that

$$
\hat{\phi}(t_i) = \Delta\omega\tau + \hat{\phi}(t_{i-1}), \quad (3)
$$

where $\Delta\omega = \omega - \hat{\omega}$ and $\tau = t_i - t_{i-1}$. From (3), one can recognize that if $\Delta\hat{\phi} \neq 0$, then there is a frequency estimation error. Hence, one can utilize $\Delta\hat{\phi}$ in making $\hat{\omega}$ track $\omega$. The basic idea for updating $\hat{\omega}$ is to employ a PI regulator such that $\Delta\hat{\phi}$ is regulated to a zero value. Then, we claim that the output of the PI regulator can be used for $\hat{\omega}$. Fig. 2 shows the block diagram of the phase angle and the frequency estimation algorithm.
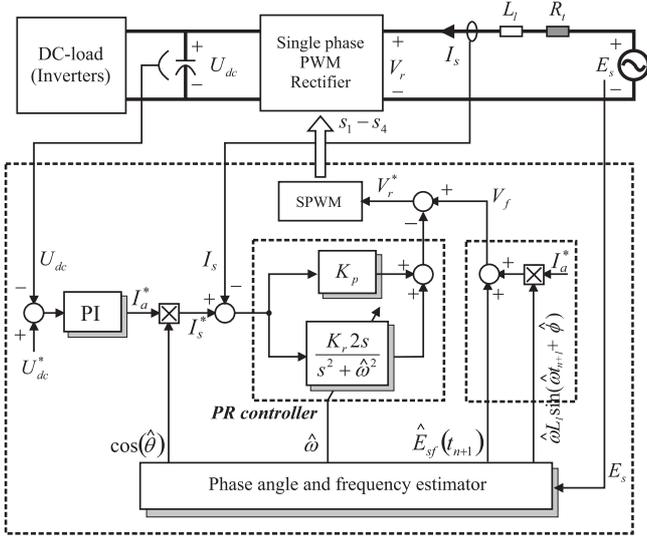
Fig. 3. Proposed controller for a single-phase PWM rectifier where $\hat{E}_{sf} = |\hat{E}_d + j\hat{E}_q|$ is the estimated fundamental component of the source voltage. The effect of $L_m$ is ignored for the convenience.

## B. DC-link and Current Controller

The structure of the proposed controller is shown in Fig. 3, which consists of a DC-link voltage controller, a current controller, and a feed-forward compensator. The source current reference is constructed such that

$$I_s^* = \cos(\hat{\theta}) \times (PI)(U_{dc}^* - U_{dc}), \qquad (4)$$

where $(PI)(\zeta)$ is the PI controller output with respect to the input $\zeta$, and $\hat{\theta}(=\omega t + \hat{\phi})$ is the estimated phase angle of the source voltage given by the phase angle estimator. Note that the current command $I_s^*$ is a 50Hz or 60Hz AC sinusoidal signal in the steady state. The control bandwidth, therefore, needs to be large enough to accommodate the 50Hz or 60Hz command. However, in a practical situation, there are sampling effect, quantizing effect, one-step delay, and the limit in the PWM frequency. Due to such physical limits, a high gain may cause instability, and thus the current bandwidth cannot be easily extended. Although the bandwidth is larger than 60Hz, a significant amount of the phase delay at 60Hz results in imperfect tracking. In this work, we used the proportional-resonant (PR) controller whose transfer function is given by [1]

$$G_r(s) = K_p + \frac{K_r 2s}{s^2 + \omega^2}, \qquad (5)$$

where $K_p$ and $K_r$ are the proportional- and the resonant-control gain, respectively, $\omega$ is the fundamental angular frequency of the source current. Note that the second term in (5), $K_r 2s/(s^2 + \omega^2)$ has the characteristics of a generalized integrator in a stationary frame [1]. Its output is in phase with the input signal, but the amplitude is amplified with time. In other words, the generalized integrator makes the amplitude gain at the resonant angular frequency $\omega$ infinite. Therefore, with the resonant control method, one can track the high frequency sinusoidal current command without increasing the switching frequency nor adopting a
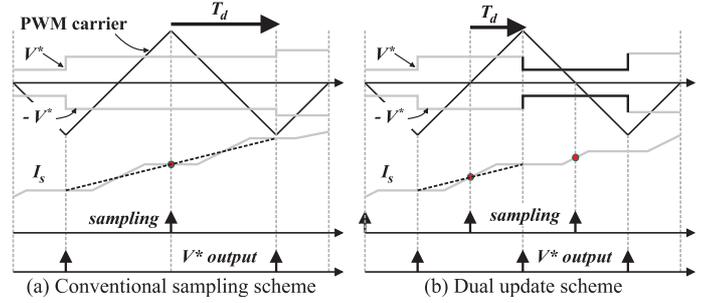


Fig. 4. Sampling instance and the control time delay $T_d$ of : (a) the conventional method and (b) the proposed double update method.
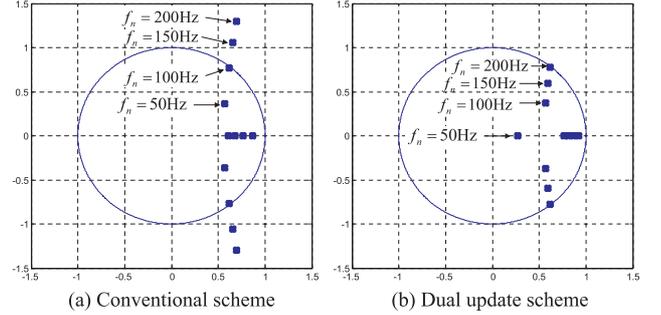


Fig. 5. Root locus of (a) the conventional method and (b) the proposed double update method with 1.5kHz switching frequency, where $f_n$ is the natural frequency of the system.

extremely large control gain that may result in a risk of systems's instability.

## C. Delayless Feed-forward Compensation

A feed-forward compensator is used to reduce the control error at the beginning and the instance when the source voltage $E_s$ changes abruptly. However, if one uses the measurement of $E_s$ for the feed-forward compensation, the compensating voltage $V_f$ includes the harmonic component of $E_s$ and measurement noise. Moreover, $V_f$ is realized after a sampling period in a digital control system. Thus, $V_f$ including a delayed harmonic signal may induce additional high frequency harmonic currents.

Assuming that $I_s = I_a \cos(\omega t + \phi)$ and the effects of the mutual inductance of the transformer $L_m$ is negligible, the current dynamic equation is given by

$$
\begin{aligned}
E_s - V_r &= L_l \frac{dI_s}{dt} + (R_{t1} + R_{t2})I_s, \\
&= L_l \frac{dI_a}{dt} \cos(\omega t + \phi) + R_t I_s \\
&\quad -\omega L_l I_a \sin(\omega t + \phi), \qquad (6)
\end{aligned}
$$

where $V_r$ is the input terminal voltage of the rectifier, $R_t = R_{t1} + R_{t2}$, and $I_a$ is the amplitude of $I_s$. One can construct a feed-forward compensator based on (6) by adding $V_f$ to the output of the current controller as shown in Fig. 3 such that

$$V_r^*(t_{n+1}) = -(PR)\big(I_s^*(t_n) - I_s(t_n)\big) + V_f(t_{n+1}), \qquad (7)$$

where $(PR)(\zeta)$ is the PR controller output with respect to the input $\zeta$. The feed-forward compensation voltage $V_f$

should consist of $E_s$ and $\omega L_l I_a \sin(\omega t + \phi)$ based on (6). In this work, to avoid the inclusion of a delayed signal and harmonic components, we use the estimated source voltage and current command for the feed-forward compensation such that

$$V_f(t_{n+1}) = \hat{E}_{sf}(t_{n+1}) + \hat{\omega} L_l I_a \sin(\hat{\omega} t_{n+1} + \hat{\phi}(t_n)), \quad (8)$$

where

$$\hat{E}_{sf}(t_{n+1}) = \left| \hat{E}_d(t_n) + j\hat{E}_q(t_n) \right| \cos\left( \hat{\omega} t_{n+1} + \hat{\phi}(t_n) \right). \quad (9)$$

Note from (9) that the estimated fundamental source voltage $\hat{E}_{sf}$ is the one step predicted value. Note also that the second term in the right side of (8) cancels out the steady state term, and thus (6) is turned to be such that

$$L_l \frac{dI_a}{dt} + R_t I_a = K_p\, e + K_r \int e\, dt, \quad (10)$$

where $e = I_a^* - I_a$ and $(\frac{2s}{s^2+\omega^2})e\cos(\omega t) = \int e\, dt \cos(\omega t)$ [1]. Note that (10) is the standard form of the PI controller with $Ls+R$ load, and one can apply the existing PI gain tuning formula to this current controller. For the gain margin $A_m$ and the phase margin $\theta_m$, the control gains can be determined according to the PI gain tuning formula [5,6] such that

$$K_p = \frac{\omega_p L_l}{A_m}, \quad (11)$$

$$K_r = K_p \left( 2\omega_p - \frac{4\omega_p^2 T_s}{\pi} + \frac{R_t}{L_l} \right), \quad (12)$$

where $\omega_p = \left(A_m\theta_m + A_m\left(A_m - 1\right)\pi/2\right)/(A_m^2 - 1)T_s$. For example, for $Am = 3$ and $\phi_m = \pi/3$ that are the generally recommended value in the literature [5,6], $K_p = 0.7775$ and $K_r = 12.2522$ with the parameters $L_l = 0.495$mH, $R_t = 7.8$m$\Omega$, $T_s = 1/3000$s.

### D. Double Update Scheme

To extend the control bandwidth without increasing the switching frequency, we decrease the control time delay by performing the measurement and the control calculation twice in a switching period, namely, *dual update scheme*. When one uses the conventional sinusoidal PWM with unipolar voltage switching [7], the output voltage is given according to the modulation index $m$ such that

$$V_r = \text{sgn}(m) \cdot V_{dc}, \quad \left(\frac{1-|m|}{4} \le \frac{t_m}{T_p} < \frac{1+|m|}{4}\right),$$
$$\text{or}\ \left(\frac{3-|m|}{4} \le \frac{t_m}{T_p} < \frac{3+|m|}{4}\right), \quad (13)$$
$$V_r = 0, \quad \text{otherwise},$$

where $m \in [-1,1]$ is the modulation index. From (13), we can obtain the current equation such as (14)(please see the next page) where $m_1$ and $m_2$ are the modulation index in the pre-half period and the post-half period, respectively. Obviously, the average value of the pre-half period and the post-half period are $\frac{V_{dc}m_1 T_p}{4L} + I_s(t_{n-1})$ and
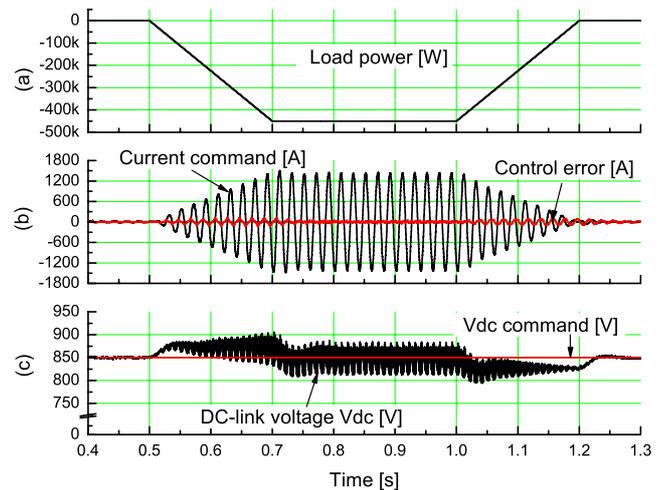


Fig. 6. Simulation result of the current control and the DC-link voltage control with an ideal voltage source under the worst load condition: (a) the load power, (b) the current command and the control error, and (c) the DC-link voltage and its command.

$\frac{V_{dc}(m_1+m_2/2)T_p}{2L} + I_s(t_{n-1})$, respectively. From (14), the instants when the current is equal to the averaged value in the each half period are obtained such that

$$t_{s1} = \frac{T_p}{4}, \qquad t_{s2} = \frac{3T_p}{4}. \quad (15)$$

Note that the sampling instant $t_{s1}$ and $t_{s2}$ are independent of $m_1$ and $m_2$. Thus, one can obtain the averaged value of the each half PWM period by measuring it at $t_{s1}$ and $t_{s2}$. Fig. 4(a) shows the PWM carrier, the output voltage command, the sampling instance, and the PWM voltage output instance of the conventional method, and Fig. 4(b) shows the same signals of the proposed double update method. One can clearly see that the control time delay $T_d$ of case(b) is the half of case(a). Fig. 5 shows the root locus of both cases with respect to the system's natural frequency. One can see from Fig. 5 that the maximum allowable control bandwidth is significantly enlarged by adopting the *dual update scheme*.

### III. SIMULATION RESULTS

Simulations were performed with the parameters given in Table I. The control gain of the DC-link voltage and the current controller were $\{K_p, K_i\} = \{4.61, 326.79\}$ and $\{K_p, K_r\} = \{0.78, 12.25\}$, respectively, and the switching frequency was 1.5kHz.

### A. Ideal Voltage Source Case

Fig. 6 shows the simulation results of the current and DC-link voltage control under an ideal voltage source condition. Fig. 6(a) shows the load power varying between 0% and $-P_{max}$ during 0.2s, which was the worst load condition in this application. Fig. 6(b) shows the current command and the control error, and Fig. 6(c) shows the DC-link voltage and its command (850V). One can see from Fig. 6 that the DC-link voltage was kept in the tolerable region even during the period of the worst load power condition, and

$$
\begin{aligned}
I_s(t) \quad &= I_s(t_{n-1}) \\
&= \mathrm{sgn}(m_1)\frac{V_{dc}}{L}\left(t - \frac{T_p(1-|m_1|)}{4}\right) + I_s(t_{n-1}) \\
&= \frac{V_{dc}m_1T_p}{2L} + I_s(t_{n-1}) \\
&= \mathrm{sgn}(m_2)\frac{V_{dc}}{L}\left(t - \frac{T_p(3-|m_2|)}{4}\right) + \frac{V_{dc}m_1T_p}{2L} + I_s(t_{n-1}), \\
&= \frac{V_{dc}(m_1+m_2)T_p}{2L} + I_s(t_{n-1})
\end{aligned}
$$

$$
\begin{aligned}
&\left(0 \le t - t_{n-1} < \tfrac{T_p(1-|m|)}{4}\right), \\
&\left(\tfrac{T_p(1-|m_1|)}{4} \le t - t_{n-1} < \tfrac{T_p(1+|m_1|)}{4}\right), \\
&\left(\tfrac{T_p(1+|m_1|)}{4} \le t - t_{n-1} < \tfrac{T_p(3-|m_2|)}{4}\right), \\
&\left(\tfrac{T_p(3-|m_2|)}{4} \le t - t_{n-1} < \tfrac{T_p(3+|m_2|)}{4}\right), \\
&\left(\tfrac{T_p(3+|m_2|)}{4} \le t - t_{n-1} < T_p\right).
\end{aligned}
\tag{14}
$$

the current was regulated perfectly, even under the low switching frequency condition such as 1.5kHz.

TABLE I

LIST OF THE SYSTEM PARAMETERS AND THEIR VALUES.

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $P_{max}$ | 450 [kW] | $U_s$ | $417 \times \sqrt{2}$ [V] |
| $\Delta P/s(max)$ | 200 [kW/s] | $U_{dc}^*$ | 850 [V] |
| $L_m$ | 100 [mH] | $L_l$ | 0.495 [mH] |
| $R_{t1}$ | 3.5 [m$\Omega$] | $R_{t2}$ | 4.3 [m$\Omega$] |
| $R_f$ | 20 [m$\Omega$] | $L_f$ | 0.317 [mH] |
| $C_f$ | 8 [mF] | $C_{dc}$ | 8.8 [mF] |

### B. Distorted and Variable Voltage Source Case

To test the immunity of the system against the source voltage's distortion and the variation, 30% THD harmonic, 25% amplitude and 120° phase angle variation were imposed to the source voltage such that

$$
\begin{aligned}
E_s \quad &= \eta417\sqrt{2}\big(\sin(\omega t + 60° + \psi) + 0.15\sin(3\omega t) + 0.08 \\
&\times \sin(5\omega t + 30°) + 0.07\sin(7\omega t - 75°)\big),
\end{aligned}
\tag{16}
$$

where $\eta \in [0.76, 1.1]$ is the amplitude variation factor and $\psi$ is the phase angle variable. In this simulation, the amplitude of $E_s$ changes from 76%($\eta = 0.76$) to 110%($\eta = 1.1$), and $\psi$ changes from 0 to 120° in a step manner at $t$=1s. Fig. 7(a)-(d) show the varying and distorted source voltage $E_s$, the estimated fundamental component of the source voltage $\hat{E}_{sf}$ and $E_s - \hat{E}_{sf}$, the current command and the control error, and the DC-link voltage and its response, respectively. Note that $\hat{E}_{sf}$ is the estimation of the fundamental component of $E_s$, thus there exist high frequency ripples in $E_s - \hat{E}_{sf}$ of Fig. 7(b). One can see from Fig. 7 that the source voltage estimator worked very well even under such a step change condition, and the proposed controller regulated the current without an erroneous behavior and kept the DC-link voltage in the tolerable region under such a highly distorted and varying source voltage condition.

Fig. 7. Simulation result of the current control and the DC-link voltage control with the distorted and variable voltage source: (a) the source voltage, (b) the estimated fundamental component of the source voltage $\hat{E}_{sf}(= E_{sf-est})$ and $E_s - \hat{E}_{sf}$, (c) the current command and the control error, and (d) the DC-link voltage and its command.

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