

**Comprehensive Investigation & Simulation of Different  
Modulation Schemes Suitable for the 3-Level T-Type Based  
Grid Side Converter**

There are various modulation schemes implemented in Grid-tied inverter for different advantages. Most commonly used modulation schemes such as symmetrical PWM and space vector PWM have the disadvantage that they do not eliminate the harmonics and sometimes they even add it (third-harmonic injection) but this can be helpful in balancing out the midpoint of the three-level T-type based inverter. This thesis is about researching and comparing new techniques in the literature and implementing at least two such modulation techniques which can be helpful in midpoint voltage balancing and subsequently coding of efficient algorithms for different modulation schemes in MATLAB/PLECS for resource optimized FPGA implementation (Zynq UltraScale+ MPSoC ZCU102).

Matlab/PLECS can be used for coding algorithms for modulation schemes.

HDL coder can be used to automatically generate the VHDL/Verilog code to implement on SoC FPGA.

**Prerequisites:**

- Strong background in power electronics
- Good programming skills in C/Matlab
- Willingness to explore and implement new ideas

**Start Date:**

01.12.2021 or later (by arrangement)

Please include your CV describing your previous experiences and transcript of records and send your application to [adeel.jamal@lea.tu-darmstadt.de](mailto:adeel.jamal@lea.tu-darmstadt.de).

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