Masterarbeit/ Master Thesis

Investigation & Analysis of Potential PLL Techniques in Continuous And Discrete Time Domain for the Synchronization of the Power Controller to the Grid Voltage During Grid Voltage Imbalances in Matlab/PLECS

PLL is an essential component of the closed-loop feedback control of Grid-tied power converters in the dq-domain. With the advancement of Inverter design techniques, PLL has also been improved and different strategies are now being employed to lock in with the grid frequency even in unsymmetrical or unbalance power system conditions and weak grids. PL-EPLL (Pseudo Linear Enhance PLL) for instance can be used to achieve Low-Voltage Ride Through (LVRT) functionality in an inverter, likewise there are many new PLL techniques proposed by researchers which have different advantages. This thesis is about researching and comparing different PLL methods being employed by researchers for catering to the problem of locking in frequency during unbalanced three-phase power system in simulation and experiment.

PLECS-RT Box would be available for testing out concepts in real-time simulations.

Siemens S120 Inverter (16kVA) is available to work on in experiemental phase.

Prerequisites:

- Working proficiency in Matlab/PLECS
- Basics of power systems and Power electronics
- Previous experience in controller design will be helpful.

Start Date:

01.12.2021 or later (by arrangement)

Please include your CV describing your previous experiences and transcript of records and send your application to adeel.jamal@lea.tu-darmstadt.de.

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